AMENDMENTS TO THE CLAIMS:

If entered, this listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1 - 16. (Canceled)

17. (Previously Presented) A MOSFET device comprising:

a gate comprising a polysilicon trace overlying a semiconductor substrate with an insulator therebetween;

a source region and a drain region in said semiconductor substrate with said polysilicon trace laterally between said source and drain regions;

a liner oxide layer overlying said polysilicon trace wherein said liner oxide layer covers sidewalls of said polysilicon trace at said source and drain regions and wherein said liner oxide layer covers the top of said polysilicon trace; and

silicon nitride spacers wherein said liner oxide layer is laterally between said silicon nitride spacers and said polysilicon trace at said source and drain regions and wherein said silicon nitride spacer

have an L-shaped profile.

18. (Original) The device according to Claim 17 wherein said liner oxide layer has a thickness of between about 50 Angstroms and 300 Angstroms.

19. (Canceled)

20. (Canceled)

21. (Previously Presented) The device according to Claim 17 wherein said silicon nitride layer is formed by one of the group of: growing by thermal process and depositing by chemical vapor deposition.

22. (Previously Presented) A MOSFET device comprising:

a gate comprising a polysilicon trace overlying a semiconductor substrate with an insulator therebetween;

a source region and a drain region in said semiconductor substrate with said polysilicon trace laterally between said source and drain regions;

a liner oxide layer overlying said polysilicon trace wherein said liner oxide layer covers sidewalls of said polysilicon trace at said source and drain regions and

wherein said liner oxide layer covers the top of said polysilicon trace; and

silicon nitride spacers wherein said liner oxide layer is laterally between said silicon nitride spacers and said polysilicon trace at said source and drain regions, wherein said silicon nitride spacers have an L-shaped profile, and wherein said silicon nitride layer is formed by one of the group of: growing by thermal process and depositing by chemical vapor deposition.

23. (Previously Presented) The device according to Claim 22 wherein said liner oxide layer has a thickness of between about 50 Angstroms and 300 Angstroms.

24. (Canceled)

25. (Canceled)

26. (Previously Presented) A MOSFET device comprising:

a gate comprising a polysilicon trace overlying a semiconductor substrate with an insulator therebetween;

a source region and a drain region in said semiconductor substrate with said polysilicon trace laterally between said source and drain regions;a liner

oxide layer overlying said polysilicon trace wherein said liner oxide layer covers sidewalls of said polysilicon trace at said source and drain regions and wherein said liner oxide layer covers the top of said polysilicon trace; and

silicon nitride spacers wherein said liner oxide layer is laterally between said silicon nitride spacers and said polysilicon trace at said source and drain regions, wherein said silicon nitride spacers have an L-shaped profile, and wherein said silicon nitride layer is formed by chemical vapor deposition.

27. (Previously Presented) The device according to Claim 26 wherein said liner oxide layer has a thickness of between about 50 Angstroms and 300 Angstroms.

28. (Canceled)